Freescale Semiconductor

MPXHZ6116A Rev 2, 06/2010

Media Resistant Integrated Silicon Pressure Sensor for Measuring Absolute Pressure, On-Chip Signal Conditioned, Temperature Compensated and Calibrated

The MPXHZ6116A series pressure sensor integrates on-chip, bipolar op amp circuitry and thin film resistor networks to provide a high output signal and temperature compensation. The sensor's packaging has been designed to provide resistance to high humidity conditions as well as common automotive media. The small form factor and high reliability of on-chip integration make this sensor a logical and economical choice for the system designer.

The MPXHZ6116A series pressure sensor is a state-of-the-art, monolithic, signal conditioned sensor designed for a wide range of applications, but particularly those employing a microcontroller or microprocessor with A/D inputs. This piezoresistive transducer combines advanced micromachining techniques, thin-film metallization, and bipolar processing to provide an accurate, high level analog output signal that is proportional to the applied pressure.

Features

- Resistant to High Humidity and Common Automotive Media
- 1.43% Maximum Error over 0 to 85°C
- Temperature Compensated from -40°C to +125°C
- Durable Thermoplastic (PPS) Surface Mount Package (SSOP)
- Ideally Suited for Microprocessor or Microcontroller-Based Systems

MPXHZ6116A Series

20 to 115 kPa (2.9 to 16.7 psi) 0.399 to 4.645 V Output

ORDERING INFORMATION									
Device Name	Package	Case	# of Ports		Pressure Type			Device Marking	
Device Name	Options	No.	None	Single	Dual	Gauge	Differential	Absolute	Device Marking
Super Small Outline Package (Media Resistant Gel) (MPXHZ6116A Series)									
MPXHZ6116A6U	Rail	1317	•					•	MPXHZ6116A
MPXHZ6116A6T1	Tape & Reel	1317	•					•	MPXHZ6116A

SUPER SMALL OUTLINE PACKAGE



MPXHZ6116A6U/6T1 CASE 1317



Operating Characteristics

Table 1. Operating Characteristics ($V_S = 5.0 \text{ Vdc}$, $T_A = 25^{\circ}\text{C}$ unless otherwise noted, Decoupling circuit shown in Figure 3 required to meet electrical specifications.)

Characteristic	Symbol	Min	Тур	Max	Unit
Pressure Range	P _{OP}	20	_	115	kPa
Supply Voltage ⁽¹⁾	Vs	4.75	5.0	5.25	Vdc
Supply Current	I _S	_	6.0	10	mAdc
Full Scale Span ⁽²⁾ (0 to 85	CC) V _{FSS}	_	4.2	_	Vdc
Offset ⁽³⁾ (0 to 85	PC) V _{off}	0.335	0.399	0.463	Vdc
Sensitivity	V/P	_	44.2	_	mV/kPa
Accuracy ⁽⁴⁾ (0 to 85	PC) —	-1.5	_	+1.5	%V _{FSS}
Pressure Range	P _{OP}	20	_	115	kPa

- 1. Device is ratiometric within this specified excitation range.
- 2. Full Scale Span (V_{FSS}) is defined as the algebraic difference between the output voltage at full rated pressure and the output voltage at the minimum rated pressure.
- 3. Offset (V_{off}) is defined as the output voltage at the minimum rated pressure.
- 4. Accuracy (error budget) is the deviation in actual output from nominal output over the entire pressure range and temperature range as a percent of V_{SS} span at 25°C due to all sources of error including the following:

Linearity: Output deviation from a straight line relationship with pressure over the specified pressure range.

Temperature Hysteresis: Output deviation at any temperature within the operating temperature range, after the temperature is cycled to

and from the minimum or maximum operating temperature points, with zero differential pressure applied.

Pressure Hysteresis: Output deviation at any pressure within the specified range, when this pressure is cycled to and from minimum

or maximum rated pressure at 25°C.

Offset Stability: Output deviation, after 1000 temperature cycles, -40° to 125°C, and 1.5 million pressure cycles, with minimum

rated pressure applied.

TcSpan: Output deviation over the temperature range of 0° to 85°C, relative to 25°C.

TcOffset: Output deviation with minimum pressure applied, over the temperature range of 0° to 85°C, relative to 25°C.

Maximum Ratings

Table 2. Maximum Ratings⁽¹⁾

Rating	Symbol	Value	Units
Maximum Pressure	P _{max}	400	kPa
Storage Temperature	T _{stg}	-40 to +125	°C
Operating Temperature	T _A	-40 to +125	°C
Output Source Current @ Full Scale Output ⁽²⁾	l _o +	+0.5	mAdc
Output Sink Current @ Minimum Pressure Offset ⁽²⁾	I _o -	-0.5	mAdc

- 1. Exposure beyond the specified limits may cause permanent damage or degradation to the device.
- 2. Maximum Output Current is controlled by effective impedance from V_{out} to Gnd or V_{out} to V_{S} in the application circuit.

Figure 1 shows a block diagram of the internal circuitry integrated on a pressure sensor chip.

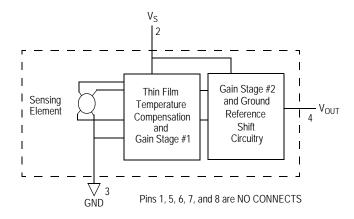


Figure 1. Fully Integrated Pressure Sensor Schematic

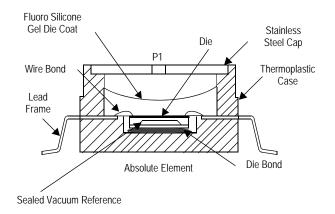
On-chip Temperature Compensation and Calibration

The performance over temperature is achieved by integrating the shear–stress strain gauge, temperature compensation, calibration, and signal conditioning circuitry onto a single monolithic chip.

Figure 2 illustrates the configuration in the basic chip carrier (case 1317) prior to porting. A gel die coat isolates the die surface and wire bonds from the environment, while allowing the pressure signal to be transmitted to the sensor diaphragm. The gel die coat and durable thermoplastic package provide a media resistant barrier that allows the sensor to operate reliably in high humidity conditions as well

as common automotive media. NOTE: The MPXHZ6116A series pressure sensor's operating characteristics, internal reliability and qualification tests are based on use of air as the pressure media. Media, other than air, may have adverse effects on sensor performance and long—term reliability. Contact the factory for information regarding media compatibility in your application.

Figure 3 shows the recommended decoupling circuit for interfacing the integrated sensor to the A/D input of a microprocessor or microcontroller. Proper decoupling of the power supply is recommended.



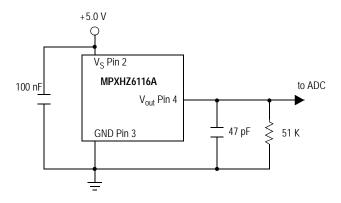


Figure 2. Cross Sectional Diagram SSOP (not to scale)

Figure 3. Typical Application Circuit (Output Source Current Operation)

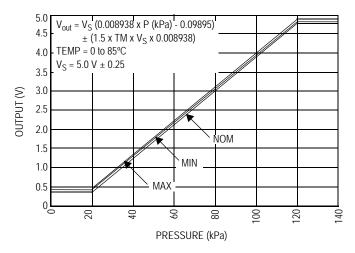
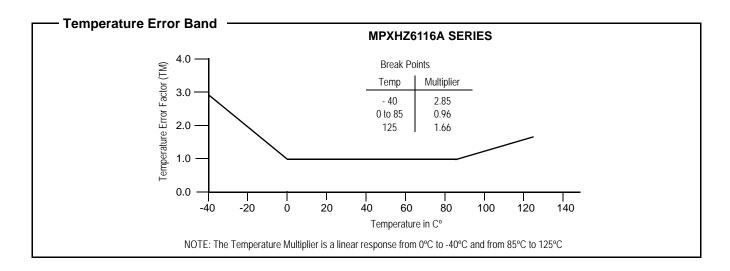
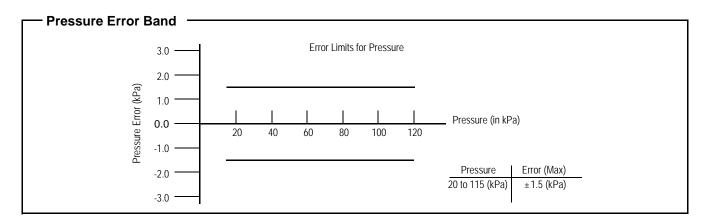


Figure 4. Output vs. Absolute Pressure





MINIMUM RECOMMENDED FOOTPRINT FOR SUPER SMALL PACKAGES

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor package must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self-align when subjected to a

solder reflow process. It is always recommended to fabricate boards with a solder mask layer to avoid bridging and/or shorting between solder pads, especially on tight tolerances and/or tight layouts.

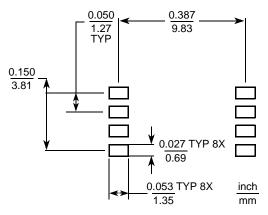
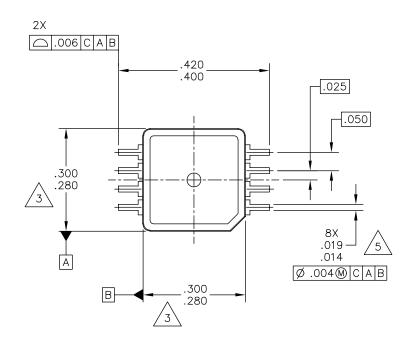
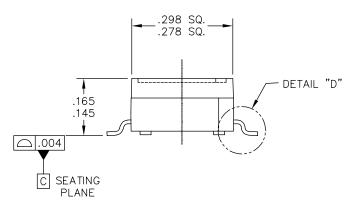


Figure 5. SSOP Footprint (Case 1317)

PACKAGE DIMENSIONS

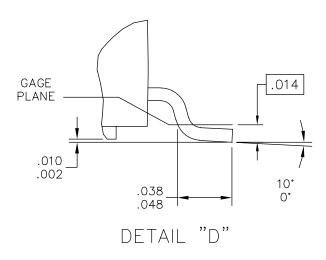




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TITLE: 8 I FAD			DOCUMENT NO: 98ARH99066A		REV: F
	SSOP		CASE NUMBER	R: 1317–04	24 MAY 2005
	3301		STANDARD: NO	DN-JEDEC	

CASE 1317-04 ISSUE F SUPER SMALL OUTLINE PACKAGE

PACKAGE DIMENSIONS



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TITLE: 8 LEAD			DOCUMENT NO): 98ARH99066A	REV: F
			CASE NUMBER	:: 1317 – 04	24 MAY 2005
	3301		STANDARD: NO	N-JEDEC	

CASE 1317-04 ISSUE F SUPER SMALL OUTLINE PACKAGE

PACKAGE DIMENSIONS

NOTES:

- 1. ALL DIMENSIONS IN INCHES.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSION SHALL NOT EXCEED .006 INCHES PER SIDE.

4. ALL VERTICAL SURFACES TO BE 5' MAXIMUM.

DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
ALLOWABLE DAMBAR PROTRUSION SHALL BE .008 INCHES MAXIMUM.

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8 LEAD SSOP			DOCUMENT NO: 98ARH99066A		REV: F
			CASE NUMBER	2: 1317–04	24 MAY 2005
			STANDARD: NO	N-JEDEC	

CASE 1317-04 ISSUE F SUPER SMALL OUTLINE PACKAGE

MPXHZ6116A

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